Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **COLLECTOR Q1**
2. **COLLECTOR Q2**
3. **EMITTER Q2**
4. **BASE Q2**
5. **SUBSTRATE**
6. **COLLECTOR Q3**
7. **EMITTER Q3**
8. **BASE Q3**
9. **BASE Q4**
10. **EMITTER Q4**
11. **COLLECTOR Q4**
12. **COLLECTOR Q5**
13. **EMITTER Q5**
14. **BASE Q5**
15. **BASE Q1**
16. **EMITTER Q1**

**.047”**

****

**.033”**

**NOTE: Substrate must be connected to the most negative point**

 **in the external circuit to maintain isolation between**

 **transistors and provide for normal transistor action.**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004 x .004”**

**Backside Potential:**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .033” X .047” DATE: 7/22/21**

**MFG: INTERSIL / RCA THICKNESS .014” P/N: CA3127**

**DG 10.1.2**

#### Rev B, 7/1